

**REMARKS**

Claims 9-20 are pending. Reconsideration of the application in light of the following remarks is respectfully requested.

**I. REJECTION OF CLAIMS 15 AND 20 UNDER 35 U.S.C. § 103(a)**

Claims 15 and 20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,792,699 (Tsui), in view of U.S. Patent No. 5,898,202 (Fulford, Jr. et al.). Withdrawal of the rejection is respectfully requested for at least the following reasons.

*i. Tsui does not disclose a dopant concentration of the bottomwall/sidewall junction capacitance reduction region peaks substantially at the bottomwall junction, as recited in claims 15 and 20.*

Claims 15 and 20 recite that a dopant concentration of the bottomwall/sidewall junction capacitance reduction region peaks substantially at the bottomwall junction. Tsui does not teach this feature as will be further appreciated below.

***The doping in Fig. 2c of Tsui does not peak substantially at the bottomwall junction, but rather near the surface of the substrate.*** In Fig. 2a, Tsui illustrates a prior art process in which field oxides 2 are grown on a silicon substrate 1. A channel layer 4 is then implanted into the substrate 1. Tsui teaches that “the peak of the channel doping profile occurs near, or a few tenths of a micron below the substrate surface.” Col. 2, lines 49-51. Because Tsui’s doping peaks near the substrate surface, Tsui does not teach a doping that peaks at the bottomwall junction as claimed. In addition, Fulford, Jr. et al. do not remedy the deficiency in Tsui, and thus claims 15 and 20, along with claim 15’s depending claims are non-obvious over the cited art. Accordingly, withdrawal of the rejection is respectfully requested.

II. REJECTION OF CLAIMS 9, 11-17, and 19-20 UNDER 35 U.S.C. § 103(a)

Claims 9, 11-17 and 19-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,792,699 (Tsui), in view of U.S. Patent No. 5,898,202 (Fulford, Jr. et al.). Withdrawal of the rejection is respectfully requested for at least the following reasons.

- i. If individually combined with Fulford et al, neither Fig. 2c of Tsui (prior art) nor Fig. 4c of Tsui (subject matter of application), teaches all limitations of claims 14, 16, and 19. Because these Figs are not combinable, claims 14, 16, and 19 are nonobvious over the cited prior art.*
  - a. The prior art discussed in Fig. 2c of Tsui does not teach a portion of the bottomwall/sidewall junction capacitance reduction region that is implanted through the gate structure, as recited in claims 14, 16, and 19.*

Each of claims 14, 16, 19, requires that at least *a portion of the bottomwall/sidewall junction capacitance reduction region is implanted through the gate structure*. Fig. 2c of Tsui (prior art) does not teach this feature as will be further appreciated below.

In discussing Fig. 2c, Tsui expressly teaches that the channel doping region 4 is implanted prior to the formation of the gate structure 6. (col 2, lines 45-55). Because the doping region 4 is implanted prior to the formation of the gate structure, Fig. 2c cannot teach a portion of the capacitance reduction region that is implanted through the gate structure. Therefore, Fig. 2c does not teach this feature and claims 14, 16, and 19 are non-obvious in view of Fig. 2c and Fulford et al.

**b. *The subject matter in Fig. 4c of Tsui does not teach a bottomwall/sidewall capacitance reduction region that extends at least partially through the bottomwall junction, as recited in claims 14, 16, and 19.***

Each of claims 14, 16, and 19 require that the bottomwall/sidewall junction capacitance reduction region extends ***at least partially through the bottomwall junction.*** Fig. 4c of Tsui (subject matter of application) does not teach this feature as will be further appreciated below.

Tsui expressly states that the barrier layer 9 "is deeper than the source/drain regions. . ." (col 5, lines 59-61). Therefore, because the barrier layer is deeper than the source/drain regions, Tsui does not teach a bottomwall/sidewall junction capacitance reduction region extends ***at least partially through the bottomwall junction.*** Therefore, Fig. 4c does not teach this feature and claims 14, 16, and 19 are non-obvious in view of Fig. 4c and Fulford et al.

**c. *In order for the cited art to meet all elements of claims 14, 16, and 19, the technologies of Fig. 2c (prior art) and Fig. 4c (subject matter of application) must be combinable. These technologies are not combinable, and therefore claims 14, 16, and 19 are nonobvious over the cited art.***

Because neither Fig. 2c nor Fig. 4c, if individually combined with Fulford et al, teaches all limitations of claims 14, 16, and 19; a motivation must be provided to combine the technology of Fig. 2c (prior art) and Fig 4c (subject matter of application). As set forth below, one of ordinary skill in the art would not modify Fig. 4c to include a barrier layer that extends through the source/drain regions as taught in Fig. 2c.

In Fig. 4c, Tsui appears to have implanted its barrier layer 9 deeper than the source/drain regions in an effort to remedy a defect with the teaching of Fig. 2c (prior art). Namely, in Fig. 2c's prior art device, annealing caused the channel implant 4 to increase its concentration at the silicon surface, giving rise to an undesirable reverse short channel effect (RSCE). See col. 3, lines 1-5. See generally, col. 1-2. By implanting the barrier layer 9 deeper than the source/drain regions (Fig. 4c, lines 59-

61), it seems likely that Tsui sought to avoid RSCE associated with Fig. 2c's technology. Therefore, one of ordinary skill in the art would not combine these technologies, let alone combine them and then additionally include the teachings of Fulford et al.

Therefore, one of ordinary skill in the art would not combine Fig. 2c (prior art) with Fig. 4c (subject matter of application), and claims 9, 15, and 17 are nonobvious over the cited prior art.

### III. CONCLUSION

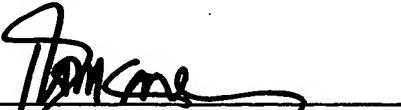
For at least the above reasons, the claims currently under consideration are believed to be in condition for allowance.

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

Should any fees be due as a result of the filing of this response, the Commissioner is hereby authorized to charge the Deposit Account Number 20-0668, TI-32513.1.

Respectfully submitted,  
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### CERTIFICATE OF MAILING (37 CFR 1.8a)

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop AF, Assistant Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date: May 19, 2006



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